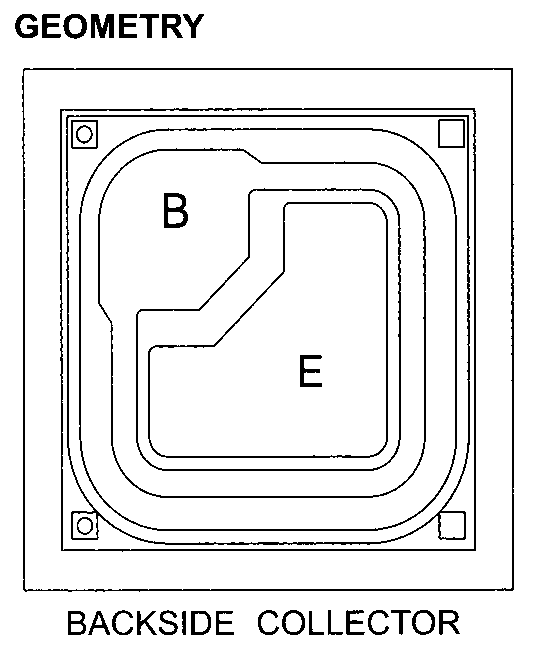
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: B = .0039” X .0039” E = .0055” X .0055”**

**Backside Potential: Collector**

**Mask Ref: CP588**

**APPROVED BY: DK DIE SIZE .015” X .015” DATE: 10/6/21**

**MFG: CENTRAL SEMI THICKNESS .009” P/N: 2N3799**

**DG 10.1.2**

#### Rev B, 7/19/02